PMU-Based Fault Location Using Voltage Measurements in Large Transmission Networks

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***Abstract*—This paper presents a general fault location method for large transmission networks which uses phasor measurement unit (PMU) voltage measurements where the injected current at a fault point can be calculated by using the voltage change and its relevant transfer impedance on any bus. A two-stage fault location optimization model is proposed, along with defining a matching degree index. The first stage is the fault region identification stage, which uses the matching degree index to determine the suspicious fault region in order to reduce the search area. The second stage is used to identify the exact fault line and fault distance. A method to determine optimal PMU placement is also proposed in this paper. Case studies verify that the proposed fault location algorithm and optimal PMU placement scheme can locate faults in large transmission networks quickly and accurately without requiring fault type classification or fault phase selection.**

***Index Terms*—Fault location, voltage measurements, optimal PMU placement, bus-impedance matrix, matching degree index.**

I. Introduction

Power system transmission lines are subjected to faults on a daily basis. Accurate fault location on a transmission line can expedite repair of the fault components, speed-up restoration, reduce outage time, and thus improve power system reliability [1].

Great effort has been made in the past to develop various algorithms for improved fault location on transmissions lines, which can be classified into either the one-terminal method [2]-[5] or the multi-terminal method [6]-[14]. One-terminal algorithms only use one terminal's voltage and the current of the fault line. However, the accuracy of these one-terminal algorithms may be adversely affected by the fault resistance and the remote terminal system's impedance. To improve the accuracy of fault location estimation, some multi-terminal algorithms have been developed which use voltages and currents—synchronously or asynchronously—from two terminals [6]-[9], three terminals [10]-[11], or even more terminals [12]-[14]. These multi-terminal methods are less influenced by the fault resistance and remote terminal system's impedance, and are theoretically more accurate.

Although existing multi-terminal algorithms can achieve high accuracy in locating faults, they are limited to fault location in a transmission network where phasor measurement units (PMU) are installed with at least one terminal for every line. Practically, PMUs cannot be installed with such density on transmission networks due to budget restrictions. For scenarios where many measurements are not available, these existing methods are no longer available. Therefore, a fault location methodology based on fewer measurements for large-scale transmission networks can be promising due to its low cost and practicality.

A number of groups have studied this capability gap [15]-[18]. A fault location method based on matching the during-fault recorded waveforms with simulated waveforms was described in [15]. However, the proposed approach needed exhaustive simulations, and was heavily dependent on the operating conditions. Based on the idea of sag contours, [16] presented a novel method using voltage measurements; however, the fault was assumed to occur at a bus, which is not typically true for practical systems. [17]-[18] have shown a more feasible method that utilized voltage measurements from one or two buses for pinpointing the location of transmission line faults, but the proposed approach has mostly depended on the assumption that the fault line was already known.

Based on the previous studies, this paper develops a universal method for locating faults in large transmission networks. It is assumed that a limited number of PMU voltage measurements are available, and the positive-sequence parameters of the network are known. This paper is organized as follows: Section II describes the basic principle of the proposed fault location method. In Section III, the implementation details of the proposed method are presented. Section IV gives three basic rules for the PMU placement scheme for the proposed method. In Section V, the implementation details of the proposed PMU placement scheme are presented. Section VI presents the test results and the performance evaluations. Conclusions are finally made in Section VII.

II. Basic Principle Of the Fault Location Method

In a n-bus transmission network, assume a fault occurs in line $i-j$ between node-i and node-j. The fault distance between the fault point node-F and node-i is xL_{ij}, where L_{ij} is the length of line $i-j$, and $0 \le x \le 1$. The positive-

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sequence network being energized by the fault current is shown in Fig. 1.

The equivalent π circuit is utilized to model the transmission lines. In Fig. 1, $Z_{L_{ij}}$ is the equivalent impedance of line $i-j$. The effect of shunt capacitances is taken into account by means of admittances $Y_{L_{ij}}$.

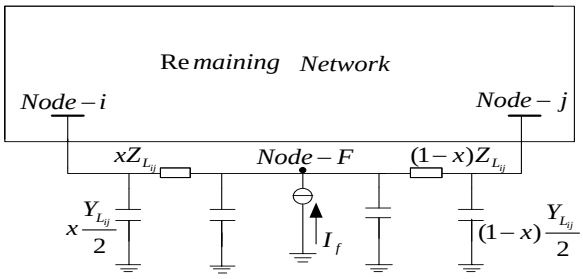

Fig. 1. Positive-sequence network during the fault.

Because the positive-sequence network is the only network existing for all types of faults, it is used for the analysis in the following discussions. All quantities, if not specifically labeled, refer to positive-sequence quantities.

In the pre-fault period, the bus-impedance matrix $\mathbf{Z}^0$ can be calculated by inverting the bus-admittance matrix Y^0 of the pre-fault network, where

$$\mathbf{Z}^0 = (Y^0)^{-1} = \begin{bmatrix} Z^0_{11} & Z^0_{12} & \dots & Z^0_{1n} \\ Z^0_{21} & Z^0_{22} & \dots & Z^0_{2n} \\ \dots & \dots & \dots & \dots \\ Z^0_{n1} & Z^0_{n2} & \dots & Z^0_{nn} \end{bmatrix}. \quad (1)$$

In the during-fault period, the fault node- F can be treated as an additional current injection bus, letting $F = n+1$. Then, a new bus-impedance matrix $\mathbf{Z}$ is obtained to represent the during-fault network. The dimension of $\mathbf{Z}$ is $(n+1)\times(n+1)$. $\mathbf{Z}$ can be derived by modifying the corresponding elements of matrix $\mathbf{Z}^0$ [19]. Then, the matrix $\mathbf{Z}$ has the form

$$\mathbf{Z} = \begin{bmatrix} Z_{11}(x) & Z_{12}(x) & \dots & Z_{1n}(x) & Z_{1(n+1)}(x) \\ Z_{21}(x) & Z_{22}(x) & \dots & Z_{2n}(x) & Z_{2(n+1)}(x) \\ \dots & \dots & \dots & \dots & \dots \\ Z_{n1}(x) & Z_{n2}(x) & \dots & Z_{nn}(x) & Z_{n(n+1)}(x) \\ Z_{(n+1)1}(x) & Z_{(n+1)2}(x) & \dots & Z_{(n+1)n}(x) & Z_{(n+1)(n+1)}(x) \end{bmatrix}. \quad (2)$$

The transfer impedances from the fault bus to other buses $Z_{i(n+1)}(x)$ $(i = 1,2...n)$ are of particular interest for fault analysis, and are helpful for estimating the fault location.

From Fig. 1, the following nodal equation can be derived:

$$\begin{bmatrix} \Delta\dot{V}_1 \\ \dots \\ \Delta\dot{V}_i \\ \dots \\ \Delta\dot{V}_n \\ \Delta\dot{V}_{n+1} \end{bmatrix} = \mathbf{Z} \begin{bmatrix} 0 \\ \dots \\ 0 \\ \dots \\ 0 \\ \dot{I}_f \end{bmatrix}. \quad (3)$$

Here, the voltage change $\Delta\dot{V}_i$ is given by

$$\Delta\dot{V}_i = \dot{V}_i - \dot{V}_i^0 \quad (4)$$

where $\dot{V}_i^0$ is the pre-fault positive-sequence voltage at bus i, $\dot{V}_i$ is the during-fault positive-sequence voltage at bus i, and $\dot{I}_f$ is the during-fault positive-sequence injected current at the fault point.

Using (2) and (3), the voltage change $\Delta\dot{V}_i$ due to the fault current $\dot{I}_f$ can be obtained by

$$\Delta\dot{V}_i = Z_{i(n+1)}(x)\dot{I}_f. \quad (5)$$

The current injection $\dot{I}_f$ is then derived as follows:

$$\dot{I}_f = \Delta\dot{V}_i / Z_{i(n+1)}(x). \quad (6)$$

From (6), the fault current injection $\dot{I}_f$ can be calculated by using the voltage change on any bus and its relevant transfer impedance.

Suppose two PMUs are installed on two buses, k and l. The fault current injection $\dot{I}_f$ calculated from these two buses should be equal, i.e.:

$$\Delta\dot{V}_k / Z_{k(n+1)}(x) = \Delta\dot{V}_l / Z_{l(n+1)}(x). \quad (7)$$

Assuming there are m PMUs available in the transmission network, the following equations can be established on the fault bus, similar to (7):

$$K_{D_1} = K_{D_2} = \dots = K_{D_m} \quad (8)$$

where K_{D_i} is defined as

$$K_{D_i} = \left|\Delta\dot{V}_{D_i} / Z_{D_i(n+1)}(x)\right|. \quad (9)$$

where $D_i (i = 1, 2, \dots, m)$ represents the bus where a PMU is placed.

It can be seen from (9) that K_{D_i} is only dependent on the measured voltage change and transfer impedance, and the latter is the function of the fault location variable x. In other words, K_{D_i} is independent of fault resistance, fault type and the pre-fault loading condition. Therefore, K_{D_i} is a function of fault distance x, where

$$K_{D_i} = K_{D_i}(x) \quad (0 \le x \le 1). \quad (10)$$

In this paper, K_{D_i} is defined as the fault location factor, which provides an efficient index for locating the fault position in the transmission network.

Based on the above analysis, the fault location problem can be modeled as nonlinear equation (8) for a transmission network with m PMUs. By solving the nonlinear equations of (8) directly, we can obtain the unknown variable x. However, the following difficulties should be considered: Equation (8) is typically a complex equation; and it is difficult for all K_{D_i} to be strictly equal due to measurement and computational errors.

In order to overcome the above difficulties, we define a matching degree δ, which is a function of fault distance x

$$\delta = \sqrt{\frac{1}{m}\sum_{i=1}^{m}\left[K_{D_i}(x) - \overline{K}(x)\right]^2} \quad (11)$$

where $\overline{K}(x)=\frac{1}{m}\sum_{i=1}^{m}K_{D_i}(x)$, $0\le x\le 1$.

Theoretically, the matching degree δ equals to zero only at the exactly fault point. However, this may not happen because of errors in measurements and computational processing. Therefore, the fault location problem is modeled as a one-dimension optimization problem where

$$\min_x \delta=\sqrt{\frac{1}{m}\sum_{i=1}^{m}\left[K_{D_i}(x)-\overline{K}(x)\right]^2}. \qquad (12)$$

The optimal solution x^* of (12) can thus be obtained by searching all the lines in the network.

III. Detailed Implementation Of The Proposed Approach

The overall flowchart of the proposed fault location algorithm is shown in Fig. 2. This algorithm consists of two stages:

Stage 1: Fault region identification.

Stage 2: Exact fault location.

Stage 1 is used to find the suspicious fault region. Stage 2 is used to find the exact fault position by searching all possible fault lines in the suspicious fault region.

Stage 1: Fault region identification

For a large-scale transmission network, searching every transmission line is time-consuming. Hence, the purpose of Stage 1 is to narrow down the search region and reduce the search time. Fig. 3 illustrates the process of identifying the possible fault region.

In Fig. 3, the PMUs are at buses e, h, and l, and a fault has occurred at point F. From (11), the matching degree δ will be zero at the fault point F if all errors are neglected. Furthermore, it can be found that the calculated δ at bus i or j, which are near the fault point F, is close to zero, while δ at bus a or g is much larger than zero. Generally speaking, δ are small for buses which are near fault position F and are large for buses which are far from fault position F.

In order to identify the fault region, we first compute the matching degree δ at each bus in the network, and then sort these matching degrees. Several buses whose matching degrees are very small can be selected as suspicious candidates for the fault bus, and the lines connecting those suspicious buses are then considered as the fault region.

If a fault occurs at a bus such as k, from (9) the fault location factor K_{D_i} is calculated as

$$K_{D_i}=\left|\Delta\dot{V}_{D_i}/Z^0_{D_ik}\right| \qquad (i=1,2...m) \qquad (13)$$

where $Z^0_{D_ik}$ is the (D_i,k) element of the pre-fault impedance matrix $\mathbf{Z}^0$. In Fig. 3, the three PMUs are placed at buses e, h and l, so D_i=e, h, and l.

From (11) and (13), if a fault occurs at a bus such as k, then the matching degree δ_k is calculated as

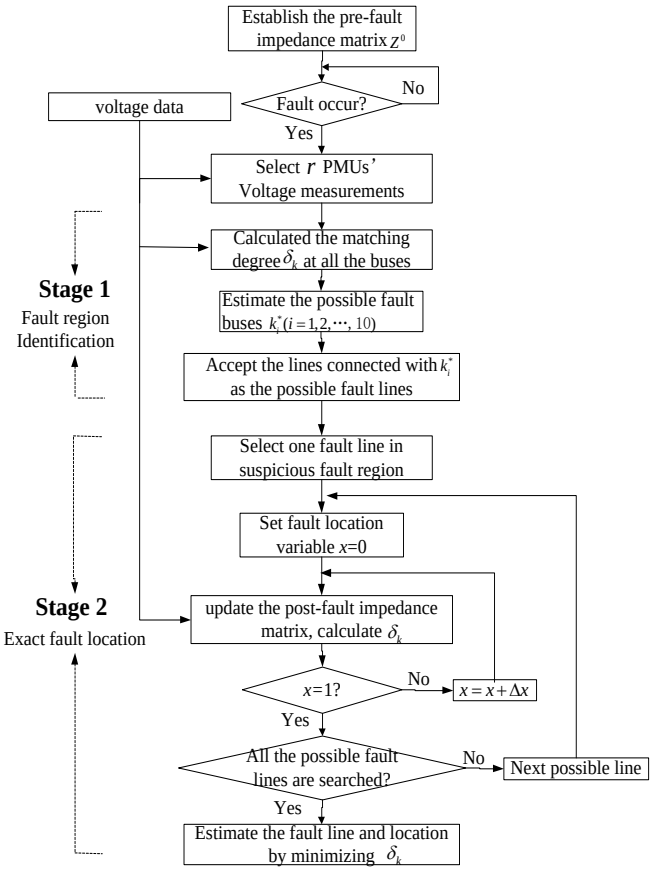

Fig. 2. The full flowchart of the proposed fault location method.

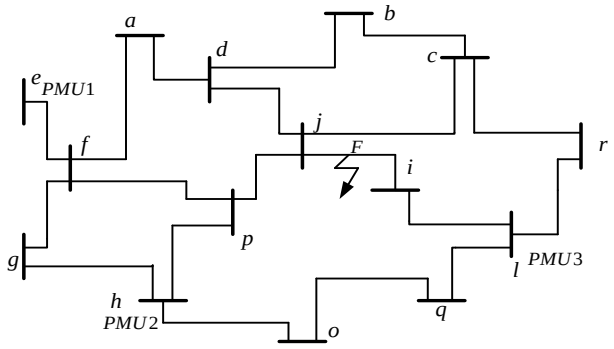

Fig. 3. Illustration of process for identifying the fault region.

$$\delta_k=\sqrt{\frac{1}{m}\sum_{i=1}^{m}\left[K_{D_i}-\overline{K}\right]^2} \qquad (14)$$

where $\overline{K}=\frac{1}{m}\sum_{i=1}^{m}K_{D_i}$.

In the case of a high impedance fault in a large system, some voltage changes may be too small, which means the estimated location may be wrong. Therefore, we only use partial PMUs' voltage measurements to calculate the matching degree instead of using all PMUs' voltage measurements in a large system. We select the data depending on the change of the bus voltage magnitude.

For a power system with n buses and m PMUs, the procedure of Stage 1 can be outlined as follows:

- After a fault is detected, the voltage data of all bus installed PMUs are obtained.
- Choose r PMUs' voltage measurements to calculate the matching degree, where r is dependent on the grid scale and the number of PMUs ($r \le m$). The standard for choosing PMU data is based on the change of bus voltage magnitude.
- Calculate the matching degree δ_k at every bus k $(k = 1, 2, ..., n)$ by using (14).
- Sort the matching degrees and select the buses k^*, whose matching degree is minimal, as the suspicious fault buses

$$k^* \in \min_k \{\delta_k\} \quad (k = 1, 2, ..., n) \tag{15}$$

- Accept the lines connected to k^* as the suspicious fault region.

To eliminate the possible effects of measurement and computational errors, we commonly choose several buses whose matching degrees are close to the minimal matching degree as the suspicious fault buses. In this case, k^* in (15) is a bus set rather than a single bus. To ensure the accuracy of the proposed algorithm, we use ten possible fault buses for a large system.

After the suspicious fault lines are identified, the exact fault point can be located quickly using Stage 2.

Stage 2: Exact fault location

Assume the suspicious fault region identified by Stage 1 includes N lines $(L_1, L_2, ..., L_N)$. Stage 2 is used to search those N lines to find the fault line and exact fault distance. The procedure of Stage 2 is as follows:

1) Let $i = 1$.
2) Select line L_i, search line L_i by a small step Δx, and calculate the matching degree $\delta_k(x)$ by using (11), where $x = k\Delta x$, $k = 1, 2, ..., 1/\Delta x$.
3) Estimate the possible fault point (L_i^*, x_i^*) by minimizing all the calculated $\delta_i(x)$ of line L_i.
4) Let $i = i + 1$, go to step 2) until $i = N + 1$.
5) Estimate the fault point (L^*, x^*) by minimizing all the calculated $\delta_i(x_i^*)$, where
   $(L^*, x^*) \in min\{\delta_i(x_i^*)\}$ $(i = 1, 2, ..., N)$.
   Here $L^* \in (L_1, L_2, ..., L_N)$, $x^* \in [0, 1]$.
6) The resulting L^* and x^* are the fault line and fault distance.

IV. PMU Placement Scheme For the Proposed Fault Location Approach

Theoretically, two voltage measurements can determine the fault location for the proposed method. However, a proper PMU placement scheme is still necessary to ensure that all possible faults can be located accurately. In our proposed PMU placement scheme, three basic rules should be followed:

Rule 1: There must be at least two PMUs in the network;
Rule 2: All terminals for each transmission line should be either directly or indirectly connected to a PMU; and
Rule 3: Constraint of n $(n \ge 3)$ edge ring circuits.

Rule 1: There must be at least two PMUs in the network.

According to the discussion in Section II, we need at least two PMUs to calculate the matching degree. If there is only one PMU, the matching degree δ decided by (11) is always zero in each line and for each distance x.

Rule 2: All terminals for each transmission line should be either directly or indirectly connected to a PMU.

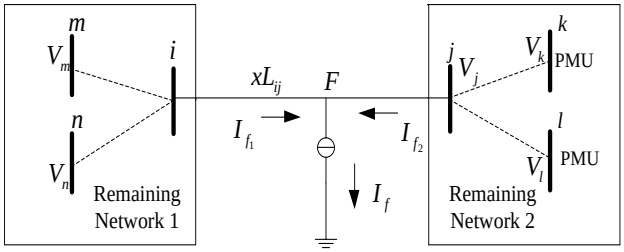

Fig. 4. Illustration of the PMU placement scheme.

In Fig. 4, we assume that the PMUs are all located in the remaining network 2, such as at k and l. For a fault occurring on line $i - j$, the fault current $\dot{I}_f$ is injected at fault point F, so both $\dot{I}_{f_1}$ and $\dot{I}_{f_2}$ are the functions of the fault location x, i.e. :

$$\dot{I}_{f_1} = g_1(x)\dot{I}_f \tag{16}$$

$$\dot{I}_{f_2} = g_2(x)\dot{I}_f \ . \tag{17}$$

Then, Fig. 4 can be separated into two parts, as shown in Fig. 5.

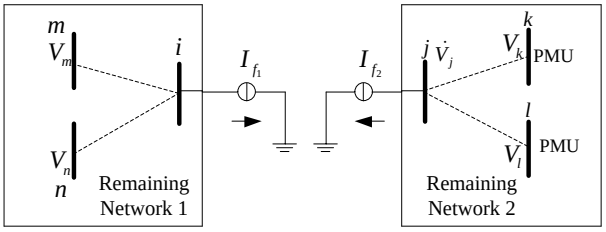

Fig. 5. The equivalent circuit of Fig. 4.

From the remaining network 2, consider that the fault occurs at bus j with a fault current of $\dot{I}_{f_2}$. Similar to (5) in Section II, the voltage change $\Delta\dot{V}_k$ on bus k is

$$\Delta\dot{V}_k = Z_{kj}\dot{I}_{f_2} \ . \tag{18}$$

Substituting (17) to (18), $\Delta\dot{V}_k$ becomes

$$\Delta\dot{V}_k = Z_{kj}g_2(x)\dot{I}_f \ . \tag{19}$$

Similar to (9), the fault location factor K_k from bus k can be obtained as

$$K_k = \left|\dot{I}_f\right| = \left|\frac{\Delta\dot{V}_k}{Z_{kj}\, g_2(x)}\right| \tag{20}$$

and similar to (20), the fault location factor K_l from bus l is

$$K_l = \left|\dot{I}_f\right| = \left|\frac{\Delta\dot{V}_l}{Z_{lj}\, g_2(x)}\right|. \tag{21}$$

From (20) and (21), we have $K_k = K_l = \left|\dot{I}_f\right|$, thus

$$\left|\Delta\dot{V}_k / Z_{kj}\right| = \left|\Delta\dot{V}_l / Z_{lj}\right|. \tag{22}$$

From (22), it can be concluded that the matching degree is always zero at any point on line $i-j$ and the fault position x cannot be obtained by solving (19). Therefore, it is impossible to locate the fault distance x on line $i-j$ when all PMUs are all located in the remaining network 2.

However, if PMUs are located in both remaining networks—for example two PMUs are placed at bus k and m —then the fault location factor K_m calculated from bus m is

$$K_m = \left|\dot{I}_f\right| = \left|\frac{\Delta\dot{V}_m}{Z_{mi}\, g_1(x)}\right|. \tag{23}$$

Because K_m varies with the fault postition x in a different function $g_1(x)$, we can identify the fault location by solving the following nonlinear equation:

$$K_m = K_k \tag{24}$$

i.e.:

$$\left|\frac{\Delta\dot{V}_m}{Z_{mi}\; g_1(x)}\right| = \left|\frac{\Delta\dot{V}_k}{Z_{kj}\; g_2(x)}\right|. \tag{25}$$

Rule 3: Constraint of n ($n \geq 3$) edge ring circuits.

The proposed algorithm will fail to determine the fault location when certain types of symmetry are present, such as a ring circuit. A node only connecting two different nodes in a ring circuit is defined as an inner node, used for describing the constraint of a ring circuit such as bus 3 in Fig. 6. A PMU must be installed on at least one of the inner nodes of a ring circuit, depending on several fundamental rules determined by results of a large number of tests.

First, we analyze the trilateral-ring circuit shown in Fig. 6. A fault on bus 3 may yield a fault location somewhere on line 1-2 if the voltage of bus 3 is unknown. Similarly, a fault on line 1-2 may cause an estimated location on line 1-3 or on line 2-3. That means faults on ring circuits cannot be estimated correctly without a PMU installed inside the ring circuit due to the complicated symmetry of the system. As a result, a PMU must be installed on bus 3 to ensure the proposed algorithm can accurately locate any faults taking place in the inner ring circuits.

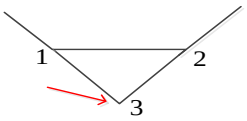

Fig. 6. The trilateral-ring circuit.

In the IEEE 39-bus system, there indeed exists a trilateral-ring circuit, which consists of buses 26-28-29 as shown in Fig. 8. In actual systems, there not only exist trilateral-ring circuits, but there also exist quadrilateral-ring circuits, five-edge-ring circuits and so on. Here we talk about a five-edge-ring circuit consisting of buses 42-43-45-44-73, which is the transmission network portion of the ZJP 76-bus—a network of Zhejiang province in China whose voltage class is equal to or higher than 525KV—shown in Fig. 10. Because this five-edge-ring circuit has four inner nodes, at least two PMUs must be installed in the four inner nodes to properly locate a fault that occurs inside the ring circuit. In Section VI, we will demonstrate the necessity of the constraint of n ($n \geq 3$) edge ring circuits.

V. Detailed Implementation Of the Proposed PMU Placement Scheme

The overall flowchart of the proposed PMU placement scheme is shown in Fig. 7. This algorithm consists of three stages:

Stage 1: place a PMU depending on rule 2. Stage 1 is used to place PMUs at buses which are located at the end of the radial network.

Stage 2: place a PMU depending on rule 3. Stage 2 is used to place a PMU at several special buses to make sure the fault location algorithm can locate the fault position accurately when faults take place in an inner ring circuit.

Stage 3: guarantee that PMU placement meets rule 1. Stage 3 is used to make sure at least two PMUs are installed in the transmission network.

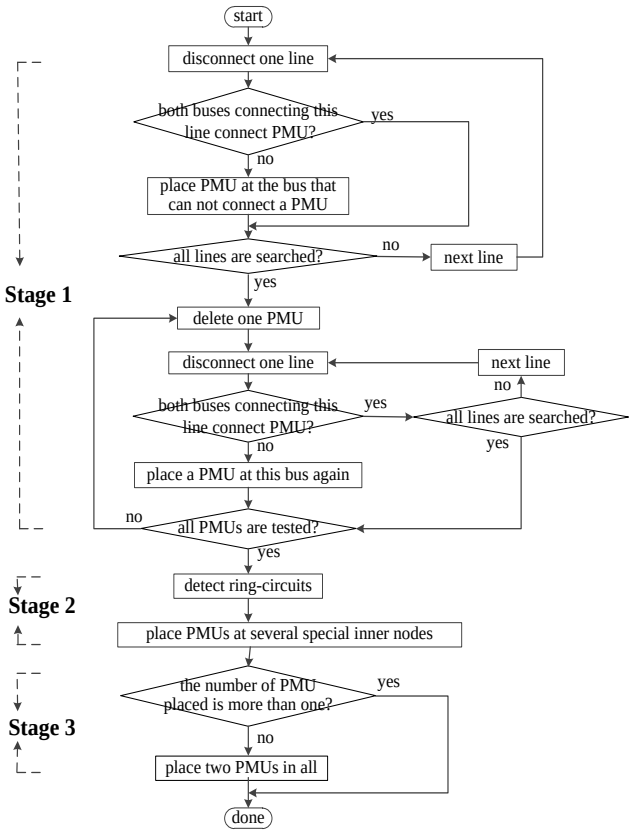

Fig. 7. The full flowchart showing the proposed PMU placement scheme.

VI. Case Studies

In order to evaluate the proposed fault location algorithm, case studies on the IEEE 39-bus system, the ZJP 76-bus system and the ZJP 543-bus system (a network of Zhejiang province in China, whose voltage class is equal to or higher than 220KV) are presented. A power system analysis software package (PSASP) [20] was utilized to obtain voltage measurements for faults of different types and locations. A large number of tests were made to ensure the validity of the proposed fault location algorithm and the PMU placement scheme. The results are shown in Table I.

TABLE I
THE RESULTS OF A LARGE NUMBER OF TESTS

System	*nb* / *nl* / *nt*	*m* / *r*	*t*	Accuracy (%)	Max error (%)
IEEE 39	39/34/12	10/10	34	100%	0.3
ZJP 76	76/84/6	21/10	84	100%	0.6
ZJP 543	543/633/61	212/35	633	100%	0.8

* *nb* denotes the number of buses.
* *nl* denotes the number of transmission lines.
* *nt* denotes the number of transformer lines.
* *m* denotes the number of PMUs installed in the tested system.
* *r* denotes the number of PMUs used to calculated the matching degree.
* *t* denotes the number of tested lines.
* Accuracy (%) denotes the location accuracy rate of all tested lines within 1% error.
* Max error denotes the maximum location error of all tested lines

From Table I, we observe that the proposed fault location algorithm can identify the fault point accurately for all tested cases. The maximal error of fault location under various fault conditions is well below 1%.

IEEE 39-bus system

To verify the efficiency of the proposed method, the well-known IEEE 39-bus test system shown in Fig. 8 was utilized. On the basis of our PMU placement scheme, 10 PMUs were installed on buses 30, 31, 32, 33, 34, 35, 36, 37, 38, and 28.

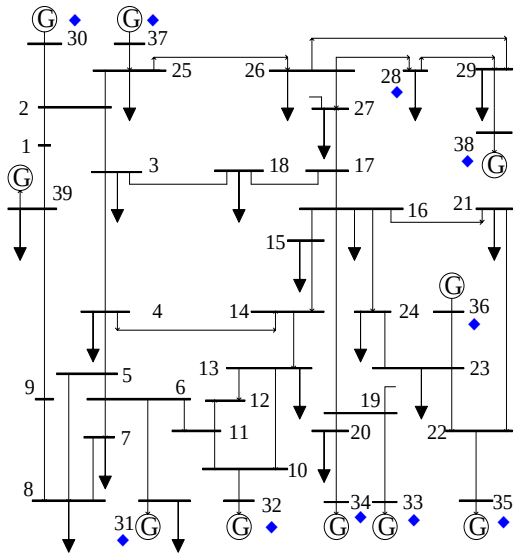

Fig. 8. The IEEE 39-bus system.

A three-phase short circuit fault at branch 24-16 with 60% branch length to bus 24 is used as an example. According to section III, the first step was to use the fault region identification stage. In this stage, the matching degrees of all buses were calculated to estimate the fault buses and the computational results are shown in Fig. 9. Note that the matching degree values are regarded as 50 when they are more than 50 in Fig. 9.

From Fig. 9, the matching degree at bus 16 is the minimal value, so the lines 16-21, 16-19, 16-17, 16-15, and 16-24 were selected as the most likely fault lines. Moreover, to ensure accuracy of the proposed algorithm, we selected ten possible fault buses including buses 16, 24, 15, 21, 17, 22, 18, 23, 19, and 27. The lines connecting those suspicious buses are then considered as the fault region.

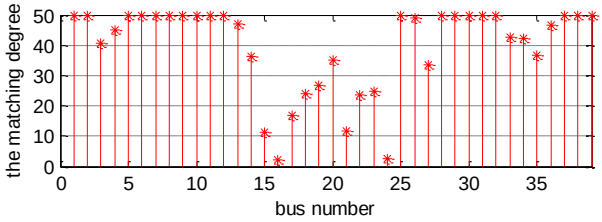

Fig. 9. Fault region identification for all buses.

TABLE II
THE FIVE MOST SUSPICIOUS LOCATIONS FOR STAGE 2

Suspicious fault locations		The matching degree	Error
line	distance		
Line 24-16	**59.9% from 24**	**0.00320**	**0.1%**
Line 21-16	88.1% from 21	0.72414	wrong
Line 19-16	100% from 19	1.99948	wrong
Line 17-16	100% from 17	1.99948	wrong
Line 16-15	0% from 16	1.99948	wrong

* wrong in the error list denotes the estimated line is not the fault line.

TABLE III
LOCATION RESULTS OF FAULTS OCCURRING IN THE INNER OF THE TRILATERAL-RING CIRCUIT IN THE IEEE 39-BUS SYSTEM

Fault location		Fault type	Bus 28 without PMU		Bus 28 with PMU	
line	distance		Estimated location		Estimated location	
26-28	45% from 26	AG	26-29	34.2%	**26-28**	**45.1%**
26-29	90% from 26	ABC	28-29	57.5%	**26-29**	**89.8%**
26-28	65% from 26	AB	26-29	49.3%	**26-28**	**64.9%**
28-29	20% from 28	ABG	26-29	80.8%	**28-29**	**20.1%**

* AG denotes A-phase to ground.
* ABC denotes three-phase short circuit to ground
* AB denotes A and B-phase short circuit.
* ABG denotes A and B-phase short circuit to ground.

After that, the exact fault location stage was performed. All the possible fault lines were searched. The five most suspicious fault locations are listed in Table II.

To validate rule 3 of the proposed PMU placement scheme, we tested faults occurring in the inner part of a trilateral-ring circuit, with the results shown in Table III. From Table III, we can see that it is essential to place a PMU at bus 28. Without a PMU installed on bus 28, the proposed algorithm cannot locate the fault position accurately because of the symmetry of this network portion.

TABLE IV
COMPUTATIONAL RESULTS UNDER DIFFERENT FAULT CONDITIONS IN IEEE39-BUS SYSTEM

Influence factors	Estimated location	Error
The parameters or values involved are totally accurate	75%	0
pre-fault PMU voltage magnitude measurement error at bus 38 is -2%	71%	4%
during-fault PMU voltage magnitude measurement error at bus 38 is -2%	82.1%	7.1%
both pre-fault and during-fault PMU voltage magnitude measurement error at bus 38 are -2%	74.6%	0.4%
Line parameter error on faulted section 4-3 is 20%	72.7%	2.3%
Line parameter error on fault neighboring section 4-14 is 20%	74.7%	0.3%

Commonly, when applying the method to practical case the various parameters or values involved will not be with high accuracy. So we give the information about the sensitivity of the proposed method in Table IV. A phase-A to ground fault occurs on the line between bus 4 and bus 3, which is 75% away from bus 4. From Table IV, we can see that the method is affected in some way, but the fault location still shows good results.

ZJP 76-bus system

To verify the efficiency of the proposed method for an actual large system, the ZJP 76-bus system shown in Fig. 10 was utilized. Twenty-one PMUs were installed on buses 4, 20, 26, 43, 44, 50, 59, 60, 61, 62, 64, 65, 66, 67, 68, 69, 70, 71, 72, 75, and 76 based on the three rules of PMU placement scheme. Some test results are shown in Table V and the results of the tests demonstrate the validity of the algorithm.

Note that when the fault line is 41-76 and there is no PMU installed on bus 76, the proposed algorithm will fail to locate the fault location. This is because the matching degree δ at any point on line 41-76 is theoretically equal to zero, which was already described in section III, and in fact all of the degrees δ are almost equal to one another and are very close to zero. In order to avoid this problem, a PMU must be placed at bus 76, which also serves to satisfy rule 2 of the PMU placement scheme.

TABLE V
SIMULATION RESULTS UNDER DIFFERENT FAULT CONDITIONS FOR THE ZJP 76-BUS SYSTEM

Fault line	Fault location	Fault type	Estimated location (%)	Error (%)
Line 18-17	45% from 23	ABG	45	0
Line 59-21	30% from 59	ABG	29.9	0.1
Line 37-36	50% from 37	AB	50	0
Line 16-62	85% from 16	AB	84.8	0.2
Line 13-14	5% from 13	AG	4.9	0.1
Line 41-76	60% from 41	AG	60	0
Line 14-12	30% from 14	ABC	30.3	0.3
Line 49-69	10% from 49	ABC	10	0

* A 0 error means that the error is less than the Δx step described in section III, which is 0.001 for this paper.

Note that buses 42, 43, 45, 44, and 73 form a five-edge-ring circuit. Several tests were made to validate the necessity of rule 3 of the proposed PMU placement scheme and the results are shown in Table VI. From Table VI we can see that at least two PMUs must be installed in the inner of the five-edge-ring circuit. Otherwise, the fault location algorithm may be wrong even with one PMU installed on bus 44. Therefore, rule 3 of the PMU placement scheme is necessary to guarantee the accuracy of the proposed fault location algorithm.

As we mentioned before, the proposed algorithm is independent of fault resistance. Here, some tests under different fault resistance conditions are made and shown in Table VII. From Table VII, we can see that the proposed algorithm can locate the fault under different fault resistance. However, the accuracy decreases when the fault resistance is very high. The reason is the voltages during the fault change little from the voltages of pre-fault. Generally, the proposed fault location algorithm is still very useful because the fault resistance is usually not high enough to invalidate it.

TABLE VI
COMPUTATIONAL RESULTS UNDER DIFFERENT PMU PLACEMENT CONDITIONS IN THE ZJP 76-BUS SYSTEM

Fault location		Fault type	NO PMU on bus 43, 44		Only bus 44 installed PMU		Both bus 43 and bus 44 installed PMU	
line	distance		Estimated location		Estimated location		Estimated location	
42-73	40% from 42	ABG	47-42	99.9%	43-42	34.6%	**42-73**	**40%**
44-45	25% from 44	AB	42-36	0.2%	44-73	26.4%	**44-45**	**24.9%**
43-45	15% from 43	AG	47-42	99.5%	42-73	80.2%	**43-45**	**55.2%**

TABLE VII
COMPUTATIONAL RESULTS UNDER DIFFERENT FAULT RESISTANCE CONDITIONS IN THE ZJP 76-BUS SYSTEM

Fault location		Fault	Errors for different fault resistance R (p.u.)						
line	distance	type	$R=0$	$R=0.01$	$R=0.02$	$R=0.05$	$R=0.1$	$R=0.5$	$R=1$
68-41	50% from 68	AG	0.1%	0	0.2%	0.1%	0.7%	4.3%	7.1%
35-34	75% from 35	ABC	0	0	0	0.3%	0.1%	1.5%	5.3%

Where $R=1$ p.u. means $R=2756.25$ ohms.

TABLE VIII
COMPUTATIONAL RESULTS UNDER DIFFERENT PMU PLACEMENT CONDITIONS IN THE ZJP 543-BUS SYSTEM

Fault location		Fault	No PMU on bus 417, 421		Only bus 417 installed PMU		Only bus 421 installed PMU		Both bus 417 and bus 421 installed PMU	
line	distance	type	Estimated location		Estimated location		Estimated location		Estimated location	
417-418	75% from 417	AG	419-420	99.3%	417-420	45.5%	420-421	13%	**417-418**	**75.2%**
417-420	35% from 417	ABG	419-420	99.1%	**417-420**	**35.1%**	418-420	64.3%	**417-420**	**35.1%**
418-420	65% from 418	ABC	419-420	99.6%	417-420	86.3%	420-421	5.1%	**418-420**	**65.3%**
418-421	25% from 418	AB	419-420	98.5%	417-420	67.2%	420-421	35.9%	**418-421**	**24.8%**
420-421	97% from 420	ABC	419-420	99.4%	418-420	66.4%	**420-421**	**96.9%**	**420-421**	**96.9%**

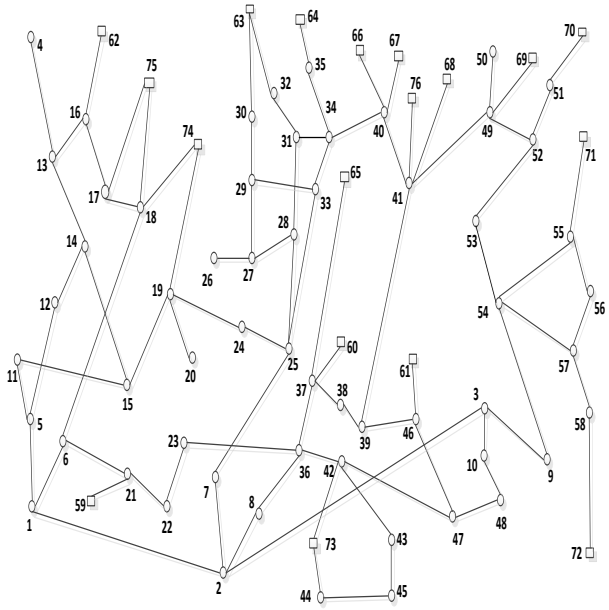

Fig. 10. The ZJP 76-bus system.

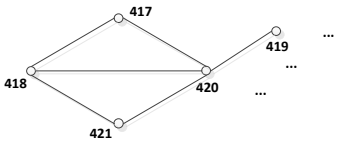

Fig. 11. Part of the network of the ZJP 543-bus system.

ZJP 543-bus system

To better evaluate the proposed algorithm, the ZJP 543-bus system was studied using our proposed method. Fig. 11 indicates part of the network of the ZJP 543-bus system. In this complicated ring network, two PMUs are installed on bus 417 and bus 421 based on the proposed optimal PMU placement scheme, which is justified by the test results shown in Table VIII. From the table we can see that the fault location cannot be located correctly without two PMUs installed on bus 417 and bus 421. Even one PMU installed on bus 417 or one PMU installed on bus 421 cannot accurately locate all faults position; in fact, in most cases they estimate the wrong fault location when faults occur in the inner ring circuits.

VII. CONCLUSIONS

This paper presents an efficient fault location method for large transmission networks. A concept of matching degree is defined which provides an efficient index to reflect the effect of fault locations. Based on this index, the proposed fault location approach uses two stages to identify the actual fault location. The distinctive features of this method are:

- A new concept of matching degree is proposed, which can provide an efficient index to reflect the effect of fault location.
- The proposed approach consists of two stages: a fault region identification stage and an exact fault location stage. The fault region identification stage is very important for large-scale power systems, and can greatly accelerate the speed of fault location.
- The proposed approach is simple and practical because it only uses voltage measurements and can be used in a large system.
- The optimal PMU placement scheme corresponding to this fault location algorithm is also given to ensure the accuracy of fault location.
- The constraint of n ($n \geq 3$) edge ring circuits for the PMU placement scheme is necessary and is first proposed in this paper.
- The proposed approach is not affected by fault resistance, fault type or pre-fault loading conditions. The proposed algorithm may be failed when the fault resistance is extremely high because the voltages during the fault may change little.

Through large tests of the IEEE 39-bus system, the ZJP 76-bus system, and the ZJP 543-bus system, we can conclude that the proposed fault location method and optimal PMU placement scheme can accurately and conveniently locate a fault.

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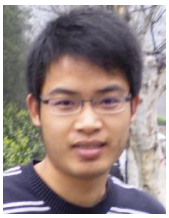

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